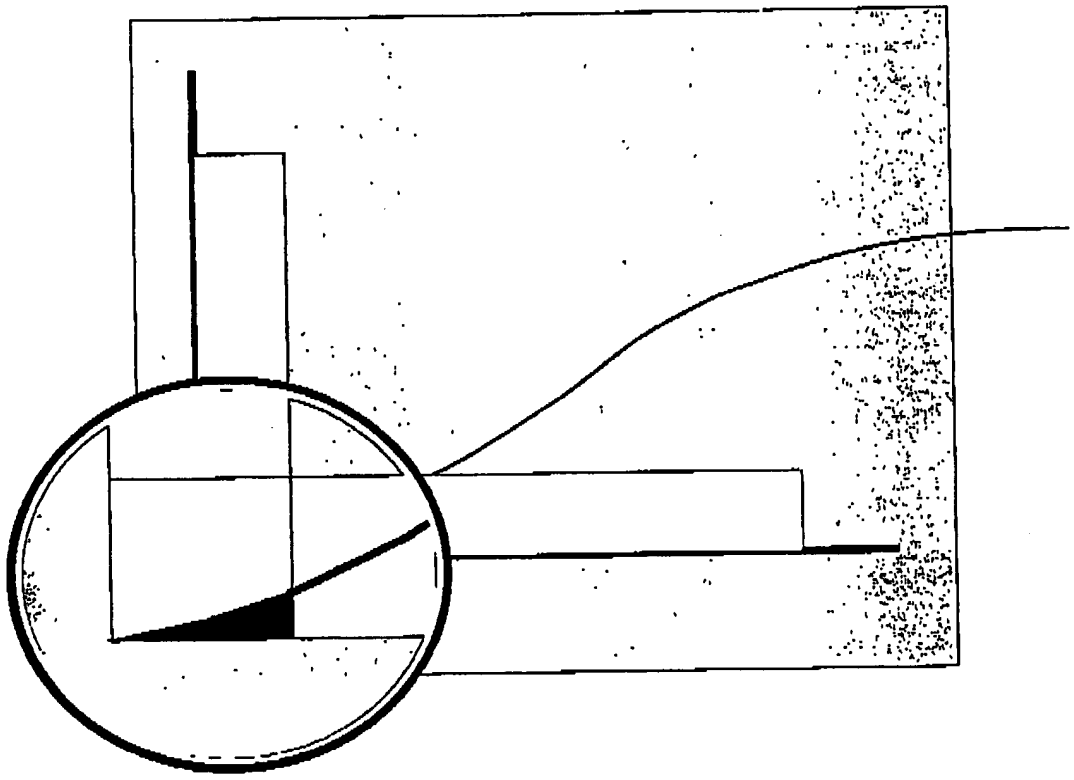
SECTION 6

DSP56156 ON-CHIP SIGMA/DELTA CODEC



SECTION CONTENTS

6.1 INTRODUCTION

This section describes the DSP56156 Sigma/Delta (ΣΔ) over sampled voice band CODEC block. It discusses the general block diagram of the A/D and D/A sections, the handshake between the DSP56156 core processor and the codec, as well as the last decimation antialiasing filter and first interpolation reconstruction filter performed in software by the DSP56156 core processor.

6.2 GENERAL DESCRIPTION

The ΣΔ over sampled voice band CODEC block is built using HCMOS technology and utilizes switched capacitor technology in some circuits. The CODEC contains one A/D converter and one D/A converter. It also contains a reference voltage generator, a bias current generator, and a master clock circuit (see Figure 6-1).

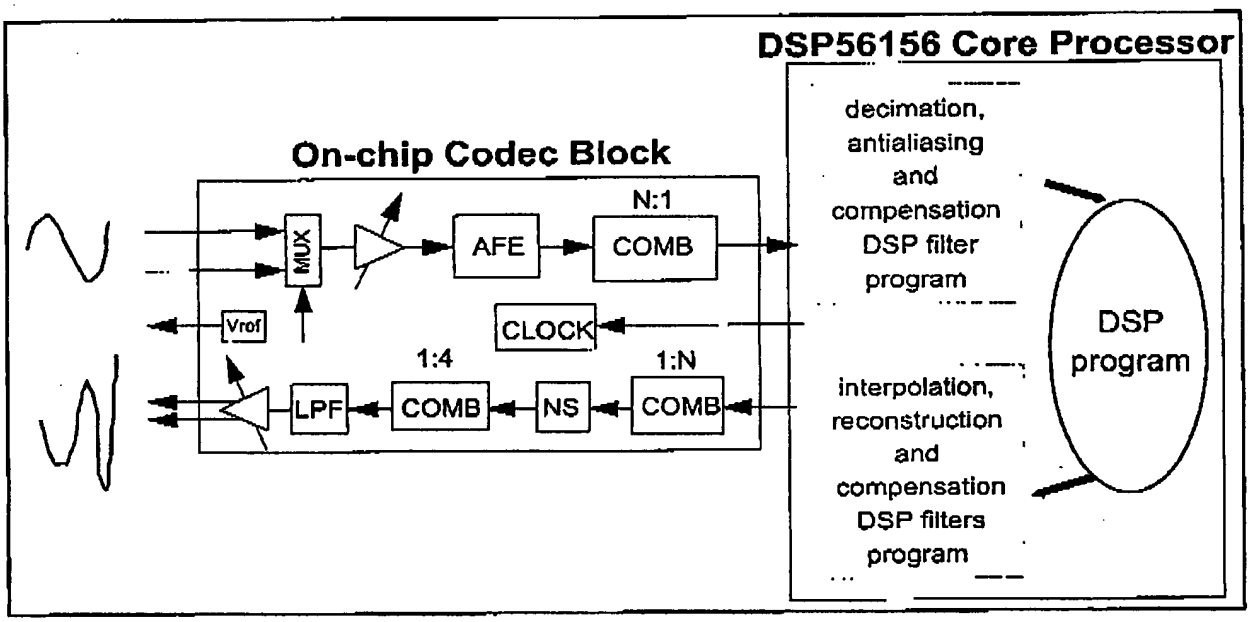


Figure 6-1 DSP56156 On-chip Sigma/Delta Functional Diagram

The A/D converter consists of an analog modulator with selectable input gain, a digital low-pass comb filter, and a parallel bus interface. The analog modulator is a second-order ΣΔ loop constructed of fully differential CMOS switched capacitor circuitry. The analog modulator input is user selectable from one of two pins. The analog modulator output is the input to a third-order digital comb filter which provides low-pass filtering and decimation. The final 16-bit result is output through a parallel interface to the DSP56156 global data bus.

The D/A converter consists of a second-order comb interpolating filter, a digital ΣΔ modulator, an analog comb decimation filter, an analog low-pass filter, a selectable attenuator, and a differential output stage. The interpolator takes in 16-bit two's complement numbers from the DSP core and up-samples them to a high frequency. The modulator changes these high frequency 16-bit words into a 1-bit stream. The switched capacitor analog filtering removes the out-of-band shaped modulator noise.

This ΣΔ codec block has been designed for maximum flexibility. The user can select one of four decimation (interpolation) ratios for the A/D (D/A) converters. Operating at a nominal sampling rate of 2 MHz, the A/D converter provides a 16-bit digital output with more than 60dB S/(N+D) for input signals in a bandwidth of 0-4 KHz. The D/A converter nominally accepts a 16-bit word at 16 KHz and has a fully differential analog output which provides more than 60dB S/(N+D) in a 0-15 KHz bandwidth, for input signals in a bandwidth of 0-4 KHz. Table 6-1 summarizes the main features of the codec block.

Table 6-1 On-chip Codec Main Features

- 16-bit resolution
- More than 60dB S/(N+D)
- Operates at sampling clock rates between 100 KHz and 3 MHz
- No off-chip components required
- Internal voltage reference (2/5 of positive power supply)
- Low power (HCMOS)

The last decimation filtering stage of the A/D section as well as the D/A first interpolation filtering stage section are implemented in software by the DSP core in order to reduce the codec cell die area.

6.3 ANALOG I/O DEFINITION

This section describes the Motorola DSP56156 analog input and output characteristics (see Figure 6-2).
There are two analog inputs MIC and AUX. Selection between MIC or AUX is made via one control bit (INS bit) and can be changed any time as desired. The electrical specifications of the two pins are identical.

The analog output consists of a fully differential driver stage, with each output having an operating range of Vref±1.0 Vp. The output op-amp is capable of driving a load of 1 kΩ in series with 50 nF between the differential outputs.

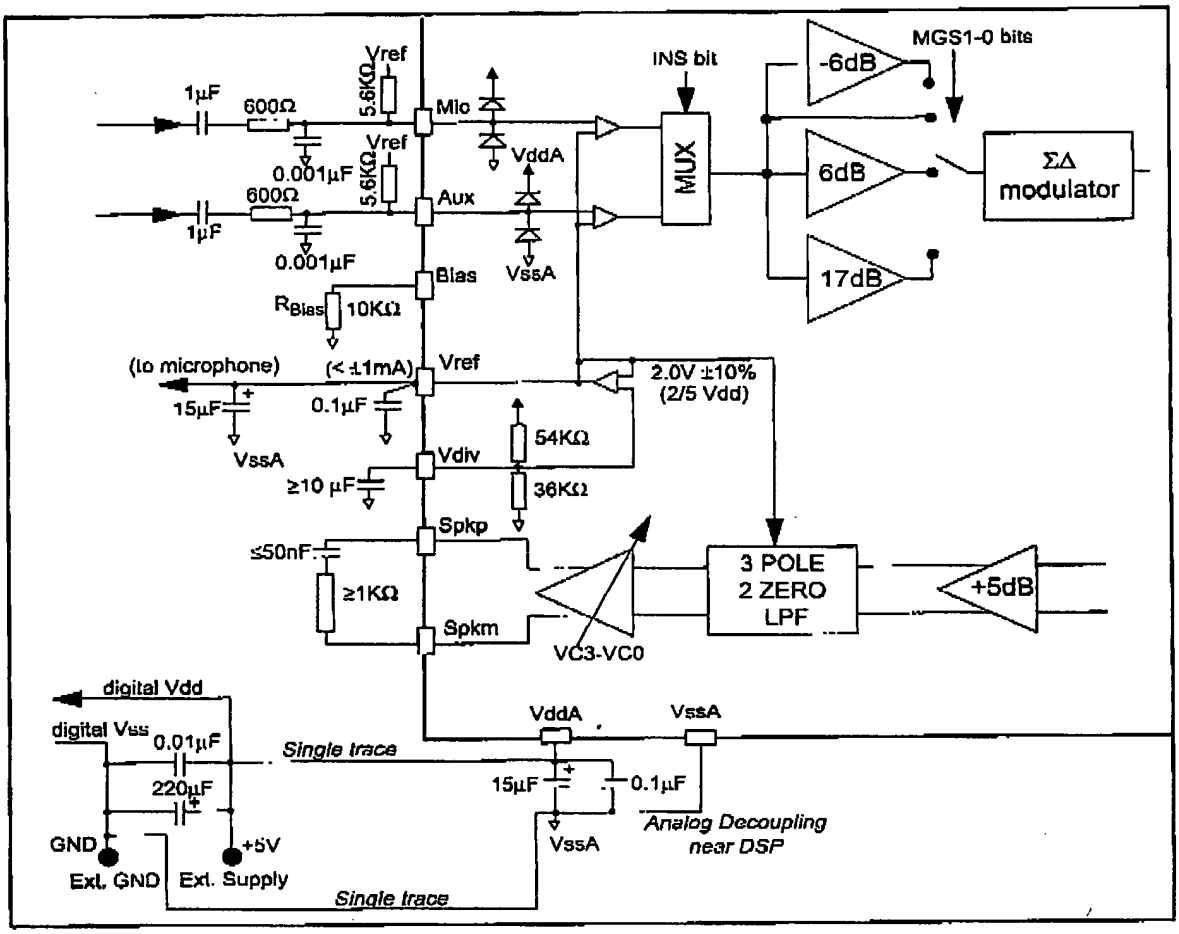


Figure 6-2 DSP56156 Analog Input and Output Diagram

6.4 INTERFACE WITH THE DSP56156 CORE PROCESSOR

This section discusses the use of each bit in the codec control registers.

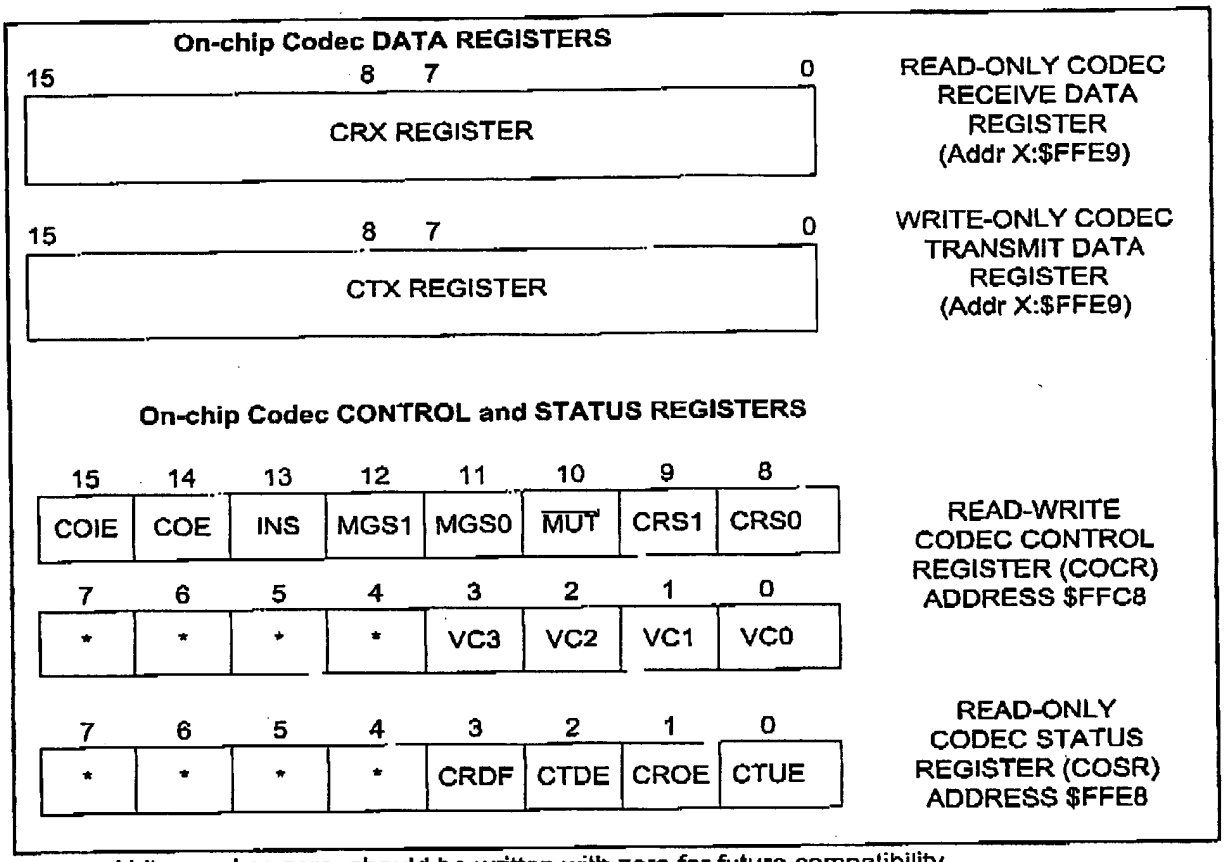
6.4.1 Interface Definition

The ΣΔ section is seen from the core as a memory mapped on-chip peripheral. Data memory locations are used for the receive data register, transmit data register, status register, and control register. One interrupt vector is assigned to the ΣΔ section.

The A/D section (receive) and the D/A section (transmit) are synchronous; that is, a common interrupt vector is used by the two sections to notify the DSP core that an input sample is to be read and/or that an output sample is to be written.

6.4.2 On-chip Codec Programming Model

Figure 6-3 shows the four memory mapped registers (mapped into three memory locations) used by the on-chip codec.



* - reserved bits, read as zero, should be written with zero for future compatibility

Figure 6-3 On-Chip Codec Programming Model

6.4.3 Codec Receive Register (CRX)

The CRX Codec Receive Register is used for A/D to DSP core data transfers. The CRX register is viewed as a 16-bit read-only register by the DSP core. The CRX register is loaded with 16-bit data from the A/D section comb filter output. This transfer operation sets the CRDF bit in the codec status register COSR. Reading CRX clears CRDF. The DSP may program the COIE bit to cause a Codec Interrupt when CRDF is set.

6.4.4 Codec Transmit Register (CTX)

The CTX Codec Transmit Register is used for DSP core to D/A data transfers. The CTX register is viewed as a 16-bit write-only register by the DSP core. Writing the CTX register

clears the CTDE bit in the codec status register COSR. The DSP may program the COIE bit to cause a Codec Interrupt when CTDE is set.

6.4.5 Codec Control Register (COCR)

The Codec Control Register COCR is a 16-bit read/write register used to direct the on-chip codec operation. The COCR bits are described in the following sections.

All COCR bits are cleared by DSP hardware and software reset.

6.4.5.1 COCR Audio Level Control Bits (VC3-VC0) Bits 0-3

Audio gain control is employed in the last stage of the on-chip codec D/A section. Bits VC0-VC2 control the volume between -20 dB and 0 dB by 5 dB steps (see Table 6-2) and VC3 is a boost bit which increases the volume level by 20 dB.

Table 6-2 Audio Level Control

VC3	VC2	VC1	VC0	Relative Level in dB
0	0	0	0	-20
0	0	0	1	-15
0	0	1	0	-10
0	0	1	1	-5
0	1	0	0	0
0	1	0	1	6
0	1	1	0	12
0	1	1	1	18
1	0	0	0	0
1	0	0	1	6
1	0	1	0	12
1	0	1	1	18
1	1	0	0	24
1	1	0	1	30
1	1	1	0	30
1	1	1	1	35

The digital reconstruction-Interpolation filter performed by the DSP core can also be used to control the output audio level in conjunction with the four VC3-VC0 bits. The gain of this filter can be adjusted in order to modify the relative level and the step between levels. Table 6-3 gives an example where the gain of the interpolation digital filter is adjusted in order to provide an output volume control between -20 dB and +35 dB in 5 dB steps.

Table 6-3 Audio Level Control with DSP Filter Gain

VC3	VC2	VC1	VC0	Relative Level dB	Digital Filter Gain	Final Output Level
0	0	0	0	-20	0	-20
0	0	0	1	-15	0	-15
0	0	1	0	-10	0	-10
0	0	1	1	-5	0	-5
0	1	0	0	0	0	0
0	1	0	1	6	-1	5
0	1	1	0	12	-2	10
0	1	1	1	18	-3	15
1	0	0	0	0	0	0
1	0	0	1	6	-1	5
1	0	1	0	12	-2	10
1	0	1	1	18	-3	15
1	1	0	0	24	-4	20
1	1	0	1	30	-5	25
1	1	1	0	30	0	30
1	1	1	1	35	0	35

6.4.5.2 COCR Codec Ratio Select Bits (CRS1-0) Bits 8,9

The Codec Ratio Select Bits are used by the DSP core to program the decimation and interpolation ratio of the on-chip codec comb filter sections. As shown in Table 6-4, the value selected as decimation and interpolation ratio also affects the DC gain of the comb filter in the A/D and D/A sections. The overall DC gain of the A/D and D/A sections is discussed in detail Sections 6.5.1 and 6.5.2.

Table 6-4 Decimation/Interpolation Ratio Control

CRS1	CRS0	Decimation Interpolation Ratio Rate	A/D Comb Filter DC Gain		D/A Comb Filter DC Gain	
0	0	125	$125^3/2^{21}$	-0.618 dB	125/128	-0.206 dB
0	1	128	1	0 dB	1	0 dB
1	0	105	$2(105^3)/2^{21}$	0.859 dB	105/128	-1.720 dB
1	1	81	$2(81^3)/2^{21}$	0.118 dB	81/128	-3.974 dB

6.4.5.3 COCR Mute Bit ($\overline{\text{MUT}}$) Bit 10

The mute bit is used to mute the output signal. When the $\overline{\text{MUT}}$ bit is cleared, the output signal is muted. When the $\overline{\text{MUT}}$ bit is set, the output signal is not muted.

6.4.5.4 COCR Microphone Gain Select Bits (MGS1-0) Bits 11,12

The Microphone Gain Select Bits are used by the DSP core to program the analog input gain. The values are given in Table 6-5. The analog modulator is guaranteed to be linear

up to 3dB below the full scale saturation values. The full scale saturation analog values result in a maximum digital A/D output ($7FFF) when the A/D comb filter has a unity gain.

Table 6-5 Microphone Gain Control

MGS1	MGS0	Gain		Modulator full scale	Full scale linearity
		Actual	dB		
0	0	0.5	-6	2 Vp	1.414 Vp
0	1	1	0	1 Vp	0.707 Vp
1	0	2	6	500 mVp	354 mVp
1	1	7.07	17	141 mVp	100 mVp

6.4.5.5 COCR Input Select Bit (INS) Bit 13

The input select bit is used by the DSP to select between the two inputs MIC and AUX. When INS is cleared, MIC is selected and when INS is set, AUX input is selected.

6.4.5.6 COCR Codec Enable Bit (COE) Bit 14

The Codec Enable Bit enables the on-chip codec section. When this bit is cleared the section is disabled and put in the power down mode. Setting the bit wakes-up and enables the on-chip codec section.

6.4.5.7 COCR Codec Interrupt Enable Bit (COIE) Bit 15

The Codec Interrupt Enable Bit enables the on-chip codec interrupt. When this bit is cleared the interrupt is disabled. Setting this bit enables the interrupt.

6.4.5.8 COCR Reserved Bits (Bits 4-7)

These bits are reserved. They should be written as zero by the user program and will read as zero.

6.4.6 Codec Status Register (COSR)

The Codec Status Register COSR is an 8-bit read-only status register used by the DSP to interrogate the status and flags of the on-chip codec. The status bits and flag bits are described in the following paragraphs.

6.4.6.1 COSR Codec Transmit Under Run Error FLag Bit (CTUE) Bit 0

The Codec Transmit Under Run Error flag bit is set when a sample has to be transmitted to the codec section while the DSP has not yet written to the CTX transmit register (under run error). In this case, the previous sample written to the CTX register is re-transmitted to the D/A section.

Hardware and software reset and STOP reset clear CTUE. CTUE is also cleared by reading the COSR with CTUE set followed by writing CTX. Clearing the COE bit in the COCR does not affect CTUE.

6.4.6.2 COSR Codec Receive Overrun Error Flag Bit (CROE) Bit 1

The Codec Receive Overrun Error Flag bit is set when a new sample is received from the codec section while the previous received sample in the CRX receive register has not been read by the DSP (overrun error). In this case, the previous received sample is overwritten in the CRX register.

Hardware and software reset and STOP reset clear CROE. CROE is also cleared by reading the COSR with CROE set followed by reading CRX. Clearing the COE bit in the COCR does not affect CTUE.

6.4.6.3 COSR Codec Transmit Data Empty Bit (CTDE) Bit 2

The Codec Transmit Data Empty (CTDE) bit indicates that the D/A Transmit register CTX is empty and can be written by the DSP. CTDE is set when the CTX register is transferred to the D/A comb filter input. CTDE is cleared when the CTX register is written by the DSP. CTDE is also set entering the Codec power down mode (COE cleared) and by a DSP reset (Hardware $\overline{\text{RESET}}$ and RESET instruction) and STOP reset.

6.4.6.4 COSR Codec Receive Data Full Bit (CRDF) Bit 3

The Codec Receive Data Full (CRDF) bit indicates that the A/D Data Receive register CRX contains data from the codec A/D section. CRDF is set when data is transferred from the A/D comb filter output to the CRX register. CRDF is cleared when the CRX Register is read by the DSP. CRDF is also cleared entering the Codec power down mode (COE cleared), by a DSP reset (Hardware $\overline{\text{RESET}}$ and RESET instruction) and STOP reset.

6.4.6.5 COSR Reserved Bits (Bits 4-15)

These bits are reserved. They should be written as zero by the user program and will read as zero.

Table 6-6 On-Chip Codec Programming Model Summary

On-chip Codec STATUS REGISTERS (COSR X:$FFE8)

7	6	5	4	3	2	1	0
*	*	*	*	CRDF	CTDE	CROE	CTUE

CRDF (read-only)	0	Data From A/D not received in CRX
	1	Data From A/D received in CRX
CTDE (read-only)	0	Data in CTX has not been transferred to D/A
	1	CTX empty
CROE (read-only)	0	No Receive Overrun Error
	1	Receive Overrun Error
CTUE (read-only)	0	No Transmit Under run Error
	1	Transmit Under run Error

On-chip Codec CONTROL (COCR) X:$FFC8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COIE	COE	INS	MGS1	MGS0	$\overline{MUT}$	CRS1	CRS0	CT3	CT2	*	*	VC3	VC2	VC1	VC0

COIE	0	CODEC interrupt disabled
	1	CODEC interrupt enabled
COE	0	CODEC disabled and put in power down
	1	CODEC enabled
INS	0	MIC pin selected as A/D input
	1	AUX pin selected as A/D input
MGS1-0 Gain Select	00	MIC or AUX amplifier gain of -6 dB
	01	MIC or AUX amplifier gain of 0 dB
	10	MIC or AUX amplifier gain of 6 dB
	11	MIC or AUX amplifier gain of 17 dB
$\overline{MUT}$	0	Speaker output muted
	1	Speaker output active
CS1-CS0 Ratio Select	00	125 selected as decimation ratio for the A/D and interpolation ratio of the D/A
	01	128 selected as decimation ratio for the A/D and interpolation ratio of the D/A
	10	105 selected as decimation ratio for the A/D and interpolation ratio of the D/A
	11	81 selected as decimation ratio for the A/D and interpolation ratio of the D/A
VC3-VC0 D/A output Gain in dB	$0	-20 dB Output volume gain
	$1	-15 dB Output volume gain
	$2	-10 dB Output volume gain
	$3	-5 dB Output volume gain
	$4	0 dB Output volume gain
	$5	6 dB Output volume gain
	$6	12 dB Output volume gain
	$7	18 dB Output volume gain
	$8	0 dB Output volume gain
	$9	6 dB Output volume gain
	$A	12 dB Output volume gain
	$B	18 dB Output volume gain
	$C	24 dB Output volume gain
	$D	30 dB Output volume gain
	$E	30 dB Output volume gain
	$F	35 dB Output volume gain

6.5 ON-CHIP CODEC FREQUENCY RESPONSE AND GAIN ANALYSIS

This section discusses the DC gain and the frequency response of the A/D and D/A blocks as a function of the decimation and interpolation ratios.

6.5.1 A/D Section Frequency Response and DC Gain

The DC gain and the A/D comb filter frequency response depends on the decimation rates selected by programming bits CRS1-CRS0 in the COCR. Table 6-7 shows the DC gain of the A/D section as a function of the decimation ratio.

Table 6-7 A/D Section DC Gain

CRS1	CRS0	Decimation Ratio Rate	DC gain of the A/D section	
			dB	Actual
0	0	125	-0.618 dB	0.9313(=$125^3/128^3$)
0	1	128	0 dB	1
1	0	105	0.859 dB	1.104(=2[105^3]/128^3)
1	1	81	0.118 dB	1.0137(=4[81^3]/128^3)

Eqn. 6-1 gives the A/D transfer function and frequency response function:

Eqn. 6-1 A/D Comb Filter Transfer Function

$$H(z) = \frac{c}{128^3}\left[\frac{1-z^{-D}}{1-z^{-1}}\right]^3$$

$$F(f) = \frac{c}{128^3}\left(\frac{\sin\left(\frac{2\pi D}{2F}\times f\right)}{\sin\left(\frac{2\pi}{2F}\times f\right)}\right)^3$$

D: decimation ratio
F: ΣΔ modulator clock
c=1 for D=125,128
c=2 for D=105
c=4 for D=81

Figure 6-4 and Figure 6-5 show an example of the A/D comb filter log magnitude response using a 2.048 MHz master clock and a decimation ratio of D=128. The figures show the frequency response in the bands 0-1.024 MHz and 0-16 KHz (Figure 6-4) and in the band 0-4 KHz (Figure 6-5).

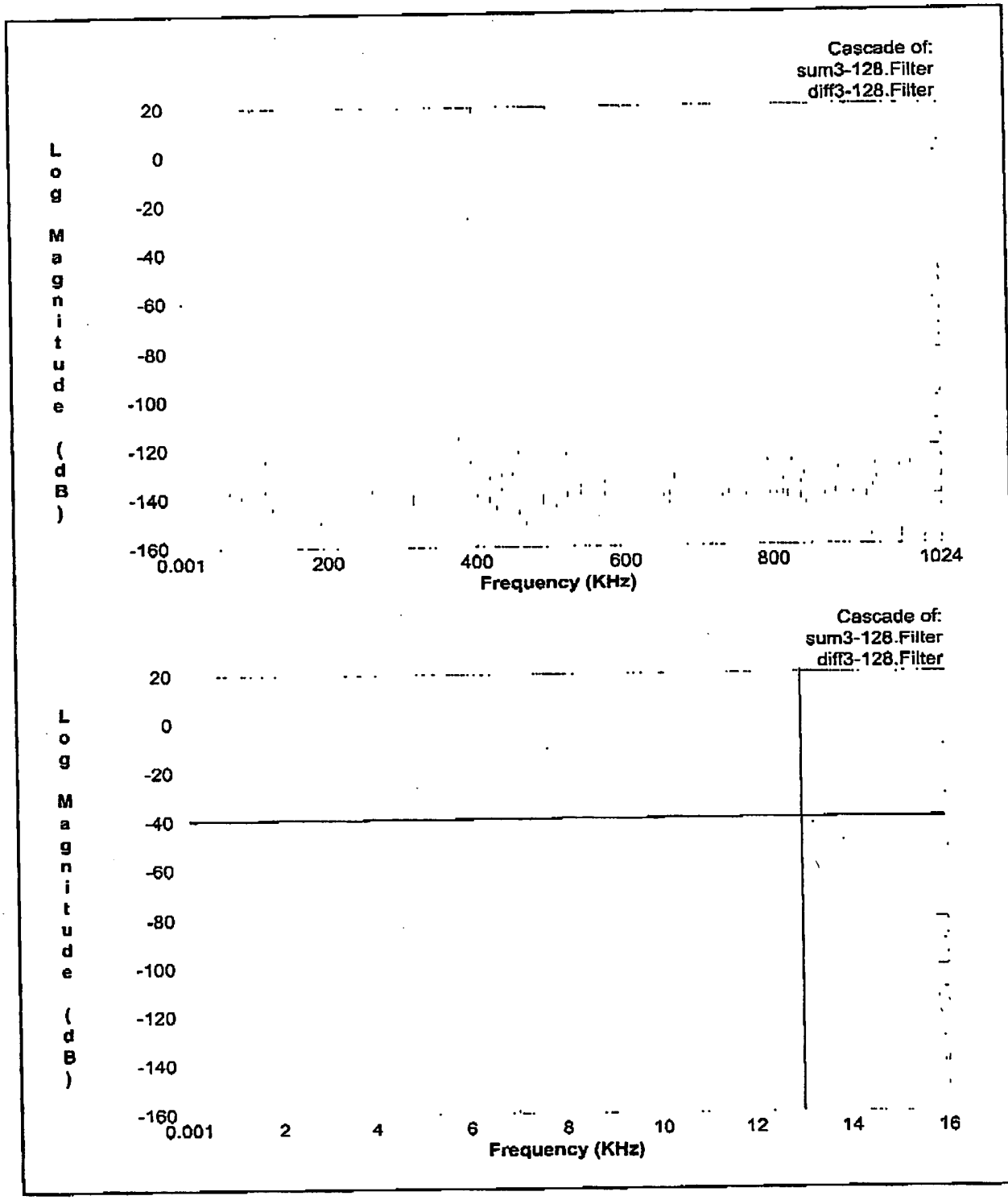


Figure 6-4 Log Magnitude Frequency Response of the A/D Comb Filter for F=2.048 MHz and D=128